Claims

We claim:

1.   A method for error protection of a cache memory, wherein each entry in the tag memory and data store within the cache memory associates with a parity bit, comprising:

    (a) providing a read request to a system memory associated with the cache memory, the read request correlating to an entry in the tag memory and the data store;

    (b) checking the parity bit associated with the correlated entry in the tag memory and the parity bit associated with the correlated entry in the data store; and

    (c) if either act (a) or act (b) indicates an error in the corresponding correlated entry, declaring a miss.

2.   The method of claim 1, wherein the cache memory is a second level cache.

3.   The method of claim 1, further comprising invalidating the correlated entry in the data store if a miss is declared in act (c).

4.   The method of claim 3, wherein act (b) comprises:

    checking the parity bit associated with the correlated entry in the tag memory; and

4   if the parity bit associated with the correlated entry

5   in the tag memory indicates no error:

6   determining if the correlated entry in the tag

7   memory indicates a hit; and

8   if there is a hit, checking the parity bit associated

9   with the correlated entry in the data store.

1   5.   The method of claim 4, further comprising:

2   if the parity bit associated with the correlated entry

3   in the data store indicates no error, retrieving the

4   correlated entry from the data store.

1   6.   The method of claim 5, wherein the retrieving the

2   correlated entry from the data store act comprises

3   retrieving the data line containing the correlated entry.

1   7.   A cache, comprising:

2   a data store;

3   a tag memory; and

4   a parity bit memory configured to store a parity bit

5   for each entry in the data store and for each entry in the

6   tag memory.

1   8.   The cache of claim 7, wherein each entry in the

2   data store has a corresponding entry in the tag memory and

3   wherein the parity bit stored for each entry in the data

4 store is independent from the parity bit for the

5 corresponding entry in the tag memory.

1   9.   The cache of claim 7, wherein each entry in the

2 data store has a corresponding entry in the tag memory and

3 wherein the parity bit memory is configured to store a

4 single parity bit for each data store entry and its

5 corresponding tag memory entry.

1   10. The cache of claim 7, wherein the cache is

2 configured as a write-through cache.

1   11. The cache of claim 7, wherein the cache is

2 configured as a write-back cache with a timeout flush.

1   .   12. The cache of claim 7, wherein the parity bit

2 memory stores a single parity bit for each cache line in

3 the data store.